

## IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled).
2. (Currently Amended) A system for verification test bench system for testing of a system-on-a-chip ~~interface of an SOC~~, said ~~verification test bench~~ system comprising:
  - ~~a verification interface model connected to said SOC interface; and~~
  - ~~a test bench external bus interface unit (EBIU) connected to said verification interface model,~~
  - ~~wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and~~
  - ~~wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model~~

said system-on-a-chip (SOC) comprising:

  - a master central processing unit (CPU) that runs test case software;
  - an SOC interface; and
  - a first external bus interface unit (EBIU) that is slaved to said master CPU; and
  - a verification test bench that is external to said SOC, said verification test bench comprising:
    - a verification interface model connected to said SOC interface; and
    - a second EBIU connected to said first EBIU and to said verification interface model, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model.
- 3-7. (Cancelled).
8. (Currently Amended) A system for verification test bench system for testing of a system-on-a-chip ~~(SOC) interface of an SOC~~, said ~~verification test bench~~ system comprising:

~~a verification interface model connected to said SOC interface; and~~  
~~a test bench external bus interface unit (EBIU) connected to said verification interface model;~~  
~~wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and~~  
~~wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC~~

said system-on-a-chip (SOC) comprising:

a master central processing unit (CPU) that runs test case software;  
an SOC interface, said SOC interface connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification interface model connected to said SOC interface by a first external bus; and

a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model.

9. (Currently Amended) The ~~verification test bench~~ system in claim 8, all the limitations of which are incorporated herein by reference, wherein ~~said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model~~ said test case software comprises software drivers.

10. (Currently Amended) The ~~verification test bench~~ system in claim 8, all the limitations of which are incorporated herein by reference, wherein registers of said SOC interface and said verification interface model are programmed by the same test case running in said SOC software.

11. (Currently Amended) The ~~verification test bench~~ system in claim 10, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes the same software driver to configure and control said SOC interface and said verification interface model.

12. (Currently Amended) The ~~verification test bench~~ system in claim 10, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes different software drivers to configure and control said SOC interface and said verification interface model.

13. (Currently Amended) The ~~verification test bench~~ system in claim 8, all the limitations of which are incorporated herein by reference, wherein said verification interface model tests an operational capability of said SOC interface.

14. (Currently Amended) The ~~verification test bench~~ system in claim 8, all the limitations of which are incorporated herein by reference, further comprising ~~at least one~~ an additional verification interface model for said verification test bench, said additional verification interface model being connected to said ~~test bench~~ second EBIU for testing additional types of SOC interfaces.

15. (Currently Amended) A system for verification ~~test bench system for testing of~~ a system-on-a-chip (SOC) interface of an SOC, said ~~verification test bench~~ system comprising:  
    ~~a verification interface model connected to said SOC interface; and~~  
    ~~a test bench external bus interface unit (EBIU) connected to said verification interface model;~~  
    ~~wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and~~  
    ~~wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC, such that said SOC interface and said verification interface model are programmed by the same test case running in said SOC~~  
    said system-on-a-chip (SOC) comprising:

a master central processing unit (CPU) that runs test case software;  
an SOC interface, said SOC interface connected to said master CPU by a first  
internal bus; and  
a first external bus interface unit (EBIU) that is slaved and connected to said  
master CPU by a second internal bus; and  
a verification test bench that is external to said SOC, said verification test bench  
comprising:  
a verification interface model connected to said SOC interface by a first external  
bus; and  
a second EBIU connected to said first EBIU by a second external bus and to said  
verification interface model by a third internal bus, wherein said second EBIU and said first  
EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said  
verification interface model are programmed by said test case software running on said master  
CPU.

16. (Currently Amended) The ~~verification test bench~~ system in claim 15, all the limitations of  
which are incorporated herein by reference, wherein said ~~SOC EBIU allows said test case~~  
~~software to control both said SOC interface and said verification interface model~~ comprises  
software drivers.

17. (Currently Amended) The ~~verification test bench~~ system in claim 15, all the limitations of  
which are incorporated herein by reference, wherein said test case software utilizes the same  
software driver to configure and control said SOC interface and said verification interface model.

18. (Currently Amended) The ~~verification test bench~~ system in claim 15, all the limitations of  
which are incorporated herein by reference, wherein said test case software utilizes different  
software drivers to configure and control said SOC interface and said verification interface  
model.

19. (Currently Amended) The ~~verification test bench~~ system in claim 15, all the limitations of which are incorporated herein by reference, wherein said verification interface model tests an operational capability of said SOC interface.

20. (Currently Amended) The ~~verification test bench~~ system in claim 15, all the limitations of which are incorporated herein by reference, further comprising ~~at least one~~ an additional verification interface model for said verification test bench, said additional verification interface model being connected to said test bench second EBIU for testing additional types of SOC interfaces.

21. (Currently Amended) A method of ~~testing~~ verification for a system-on-a-chip (SOC) ~~interface of an SOC~~, said method comprising:

~~connecting a verification interface model to said SOC interface;~~  
~~connecting a test bench external bus interface unit (EBIU) to said verification interface model;~~  
~~connecting said test bench EBIU to a SOC EBIU within said SOC; and~~  
~~comparing said SOC interface with said interface model~~  
slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC;  
connecting said SOC interface to an external verification interface model, which is external to said SOC;  
connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and  
controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC.

22. (Currently Amended) The method in claim 21, all the limitations of which are incorporated herein by reference, further comprising ~~allowing, through said SOC EBIU, a test~~

~~case running in said SOC to control both said SOC interface and said verification interface model wherein said test case software comprises software drivers.~~

23. (Currently Amended) The method in claim 21, all the limitations of which are incorporated herein by reference, further comprising programming registers of said SOC interface and said verification interface model by [[a]] the same test case ~~running in said SOC software~~.

24. (Currently Amended) The method in claim 23, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes the same software driver to configure and control said SOC interface and said verification interface model.

25. (Currently Amended) The method in claim 23, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes different software drivers to configure and control said SOC interface and said verification interface model.

26. (Currently Amended) The method in claim 21, all the limitations of which are incorporated herein by reference, ~~wherein said~~ further comprising comparing process tests said SOC interface with said verification test interface to test an operational capability of said SOC interface.

27. (Currently Amended) The method in claim 21, all the limitations of which are incorporated herein by reference, further comprising:

connecting at least one additional verification interface model to said ~~test bench~~ second EBIU; and

testing additional types of SOC interfaces.

28. (Currently Amended) A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for ~~testing verification of~~ a system-on-a-chip (SOC) ~~interface of an SOC~~, said method comprising:

- ~~connecting a verification interface model to said SOC interface;~~
- ~~connecting a test bench external bus interface unit (EBIU) to said verification interface model;~~
- ~~connecting said test bench EBIU to a SOC EBIU within said SOC; and~~
- ~~comparing said SOC interface with said interface model~~
- slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC;
- connecting said SOC interface to an external verification interface model, which is external to said SOC;
- connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and
- controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC.

29. (Currently Amended) The program storage device in claim 28, all the limitations of which are incorporated herein by reference, ~~further comprising allowing, through said SOC EBIU, a test case running in said SOC to control both said SOC interface and said verification interface model wherein said test case software comprises software drivers.~~

30. (Currently Amended) The program storage device in claim 28, all the limitations of which are incorporated herein by reference, further comprising programming registers of said SOC interface and said verification interface model by [[a]] the same test case ~~running in said SOC software.~~

31. (Currently Amended) The program storage device in claim 30, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes the same software driver to configure and control said SOC interface and said verification interface model.

32. (Currently Amended) The program storage device in claim 30, all the limitations of which are incorporated herein by reference, wherein said test case software utilizes different software drivers to configure and control said SOC interface and said verification interface model.

33. (Currently Amended) The program storage device in claim 28, all the limitations of which are incorporated herein by reference, ~~wherein said~~ further comprising comparing process tests said SOC interface with said verification test interface to test an operational capability of said SOC interface.

34. (Currently Amended) The program storage device in claim 28, all the limitations of which are incorporated herein by reference, ~~wherein said method~~ further ~~comprises~~ comprising:  
connecting at least one additional verification interface model to said ~~test bench~~ second EBIU; and  
testing additional types of SOC interfaces.